Joseph A. Fisher
Hewlett-Packard Senior Fellow (Retired)
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Education:

- PhD (Computer Science) 1979, Courant Institute of New York University.
- MS (Computer Science) 1976, Courant Institute (New York University).
- AB (Mathematics, with honors) 1968, New York University.

Experience:

Hewlett-Packard Company, 1990-2006

- Senior Fellow, Hewlett-Packard (Highest technical rank), 2002-6
- Hewlett-Packard Fellow (Fellow title instituted at HP in 2000, but at that rank for several years before).
- Director, Hewlett-Packard Laboratories Advanced Architecture research program, 2005-6.
- Director (and Founder), Hewlett-Packard Laboratories, Cambridge, MA, 1994-2003.
- Member of Hewlett-Packard's Technology Council, 2001-2.

Multiflow Computer, Inc, 1984-1990

- Founder (with 2 others) and President 1984.
- Executive Vice President 1985-90, additionally Chief Technical Officer, 1989-90.
- Member of the Board of Directors, 1984-90.

Yale University, 1979-1984

- Associate Professor of Computer Science, 1983-84.

- Assistant Professor of Computer Science, 1979-83.

Honors:

- Winner, IEEE Computer Society B. Ramakrishna Rau Award, 2012, "for the development of trace scheduling compilation and pioneering work in VLIW (Very Long Instruction Word) architectures."

- Winner, IEEE/ACM Eckert-Mauchly award (highest award in computer architecture), 2003, “In recognition of 25 years of seminal contributions to instruction-level parallelism, pioneering work on VLIW architectures, and the formulation of the Trace Scheduling compilation technique”.

- 1984 Paper in PLDI (see below) selected as one of most influential in PLDI history.

- 1983 Paper in ISCA (see below) selected as one of most influential in ISCA history.

- Eli Whitney Connecticut Entrepreneur of the Year, 1987.

- Presidential Young Investigator Award, National Science Foundation, 1984 (research grant to Yale University not started due to the transition to Multiflow).

(Representative) Professional Activities:

- Editorial Board, Computer Architecture Letters.

- Standing committee member for Embedded and Hybrid Systems, Science and Engineering Research Council, Singapore. 2002-6.

- ACM Transactions On Computer Systems (TOCS), Associate Editor, 1993-1995.

- Journal of Parallel Processing and Programming Languages, Member of the Editorial Board, since 1993.

- North American General Co-Chair, ACM-IEEE International Symposium On Computer Architecture, 1995.

- ACM-IEEE Micro (International Conference), Program Co-Chair, 2001 and Chair 1982. Program Committee, frequently.

- National Science Foundation, Division of Computer and Computation Research, Member Advisory Committee, 1987-89.

- International Journal of High Speed Computing, Member of the Editorial Board.

- National Science Foundation, Review panelist, 1983, 1985.

- ACM National Lecturer, 1981-82.

- ACM Special Interest Group on Microprogramming, Board member, 1982-84.

- Technical Committee on Microprogramming, IEEE Computer Society, Board member, 1981-2

- Program committee, many conferences.

- Organized and participated in many panels.

- Many Ph.D. committees, including those at Yale, MIT, Carnegie-Mellon.

Books

- Embedded Computing: A VLIW approach to architecture, compilers and tools. With Paolo Faraboschi and Cliff Young, Elsevier/Morgan-Kaufmann, 2004.

- Instruction-level Parallelism, A Special Issue of The Journal of Supercomputing, John Wiley, January 1993 (editor, with Bob Rau). Also published as a book by Kluwer Academic Publishers, 1993.

Journal Publications:

- Instruction Scheduling for Instruction-Level Parallel Processors, with Paolo Faraboschi and Cliff Young. Proc. IEEE, 89(11):1638-1659 (Nov 2001)

- P. Faraboschi, G. Desoli, J.A. Fisher: VLIW Architectures for DSP and Multimedia Applications -- The Latest Word in Digital and Media Processing, IEEE Signal Processing, March 1998

- Walk-Time Techniques: Catalyst for Architectural Change. Computer. V30, number 9, September, 1997.

- Instruction-Level Parallel Processing: History, Overview and Perspective. With B. Ramakrishna Rau. The Journal of Supercomputing, John Wiley, January 1993.

- Instruction-level parallelism. With B. Ramakrishna Rau. Science, 253(5025), pp. 1233-1242, September 1991. A slightly longer and more detailed version is an HP Labs Technical Report, HPL-92-02.

- Measuring the parallelism available for long instruction word architectures. With Alexandru Nicolau. IEEE Transactions on Computers. July 1984

- The VLIW machine: A multiprocessor for compiling scientific code. IEEE COMPUTER, pages 45-53. July 1984

- Microcode compaction: Extending the boundaries. With D. Landskov and B. D. Shriver. International Journal of Computer and Information Sciences, 13 (1): 1-21, 1984.

- Trace scheduling: A technique for global microcode compaction. IEEE Transactions on Computers C-30(7):478-490, July 1981.

- A simpler counterexample to the reconstruction conjecture for denumerable graphs, with R. L. Graham and F. Harary. Journal of Combinatorial Theory 12(B): 1971.

- A counterexample to the countable version of a conjecture of Ulam. Journal of Combinatorial Theory 7(4): 364-365, 1969.

Refereed Conference Papers:

- DELI: A New Run-time Control Point. With Giuseppe Desoli, Nikolay Mateev, Evelyn Duesterwald, and Paolo Faraboschi. 35th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-35) November, 2002.

- Lx: A technology platform for customizable VLIW embedded processing. With Paolo Faraboschi, Geoffrey Brown, Giuseppe Desoli, and Fred (Mark Owen) Homewood. In Proceedings of the 27th Annual International Symposium on Computer Architecture, June 2000.

- Customized Instruction-sets for Embedded Processors. 36th Design Automation Conference, New Orleans, June 1999.

- Custom-Fit Processors: Letting Applications Define Architectures. With Paolo Faraboschi and Giuseppe Desoli. In The 29th Annual International Symposium on Microarchitecture, pages 324-335. ACM and IEEE Computer Society, December 1996.

- Predicting conditional branch directions from previous runs of a program. With Stefan M. Freudenberger. Proceedings of the Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (Boston, Mass., 1992), 85-95. Also published at HP Labs Technical Report HPL-92-98

- Software techniques and tradeoffs in instruction-level parallelism. In Proceedings of the Workshop on Advanced Compilation Techniques for Novel Machine Architectures, National Science Foundation of the United States and National Council for Research and Development of Israel, June 1991. Refereed and edited monograph of invited participants to be published by Springer-Verlag.

- Supercomputing using VLIW architectures: Executing many RISC operations every clock tick. Workshop: Supercomputing Tools for Science and Engineering. Pisa, Italy, December, 1989.

- Parallel processing: A smart compiler and a dumb machine, with John R. Ellis, John C. Ruttenberg and Alexandru Nicolau. In Proceedings of the SIGPLAN '84: Symposium on Compiler Construction, pages 37-47. ACM, June 1984.

- VLIW machines: Multiprocessors we can actually program, with John J. O'Donnell. In Spring Compcon '84 pages 299-305. IEEE Computer Society, February 1984. Also available as Yale Technical Report 298, Yale University, Department of Computer Science, January 1984.

- Very long instruction word architectures and the ELI-512. In The 10th Annual International Symposium on Computer Architecture, pages 140-150. IEEE Computer Society and ACM, June 1983. Also available as Yale Technical Report 253, Yale University, Department of Computer Science, December 1982, Revised 1983.

- Lifting the restriction of aggregate data motion in parallel processing, with John Ruttenberg. In IEEE International Workshop on Computer Systems Organization, pages 211-215. IEEE Computer Society, March 1983.

- Microcode Compaction: Looking Backward and Looking Forward. With Landskov, D. and Shriver, B.D. 1981 National Computer Conference, AFIPS, 1981, pp. 95-102.

- Using an oracle to measure parallelism in single instruction stream programs. In The 14th Annual Microprogramming Workshop, pages 171-182. ACM and IEEE Computer Society, October 1981.

- 2n-way jump microinstruction hardware and an effective instruction binding method. In The 13th Annual Microprogramming Workshop, pages 64-75. ACM and IEEE Computer Society, November 1980.

(Representative) Invited Conference and Other Talks:

- Keynote Address at CASES, 2004.

- Eckert-Mauckly lecture at ISCA, June 2003.

- Crest Distinguished Lecture, Georgia Tech, 2002.

- Keynote Address, 11th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming, Atlanta, GA, May 1999.

- Keynote Address, Micro-31: ACM/IEEE International Symposium on Microarchitecture, Dallas, TX, November, 1998.

- Custom-Fit Processors, Invited talk, Princeton University, November, 1996.

- Custom-Fit Processors, Invited talk, PACT-II, October, 1996.

- Custom-Fit Processors, Keynote Address, Conference on High Performance Compuuter Architectures, February, 1996.

- Instruction-Level Parallelism. Invited Lecture, Lockheed Research Center. Palo Alto, CA, March, 1993.

- Instruction-Level Parallelism. Invited Lecture, American Institute of Physics, Annual Corporate Associates Meeting. Palo Alto, CA, October 1992.

- Mapping Ideal Instruction-Level Parallelism Into Reality. Invited address, Micro-25. Portland, OR, November, 1992.

- RISC: The Death of Microcode or The Victory of Microcode. Keynote address, Micro-24. Albuquerque, NM, November, 1991.

- Instruction-level Parallelism. Distinguished Lecture, Princeton University, September, 1991.

- VLIW architectures: An inevitable standard for the future? In Supercomputing 90, Second European Conference on Supercomputing. London, England. January, 1990.

- Microprogramming, microprocessing, and supercomputing. In 13th Annual Conference on Microprogramming and Microprocessing. Zurich, Switzerland, September, 1988 (Keynote Address and paper).

- Replacing hardware that thinks (especially about parallelism) with a very smart compiler. In International Specialist Seminar on the Design and Application of Parallel Digital Processors. The Institution of Electrical Engineers, Electronics Division (Great Britain). Lisbon, Portugal, June, 1988.

- Very Long Instruction Word architectures: Supercomputing via overlapped execution. In Proceedings of The Second International Conference on Supercomputing. International Supercomputing Institute, Santa Clara, CA, May, 1987.

- A new architecture for supercomputing. In Compcon, Spring '87. IEEE Computer Society, February, 1987.

- Wide instruction word architectures: Solving the supercomputer software problem. In Proceedings of the International Seminar on Scientific Supercomputers, pages 29-46. Institut National de Recherche en Informatique et en Automatique (INRIA). Published by North Holland, February 1987.

- Many more departmental colloquia, industrial and other invited talks.

(Representative) Technical Reports and Other Publications:

- Many Hewlett-Packard Technical Reports.

- Instruction-Level Parallelism, 90 minute video in The Distinguished Lecture Series, University Video, October, 1992.

- The awful truth about software, invited editorial in The Computer Bulletin, British Computer Society, February, 1990.

- Design and use of the Yale Digital Simulator. With Douglas Baldwin, Richard Kelsey, John Ruttenberg and John Ellis. Yale Computer Science Department Technical Report No. 267. April 1983

- Computer systems architecture at Yale. Research Report 241, Yale University, Department of Computer Science, July 1982.

- The Optimization of Horizontal Microcode Within and Beyond Basic Blocks: An Application of Processor Scheduling With Resources. PhD Thesis. Also, U.S. Department of Energy Report COO-3077-161, Courant Mathematics and Computing Laboratory, New York University, October 1979.

Ph.D. Theses Directly Supervised:

- *John Ellis.* Bulldog: A Compiler For VLIW Architectures, Yale University, May 1984. First place, ACM Distinguished Thesis Award.

- *Alex Nicolau.* Parallelism, Memory Anti-aliasing and Correctness Issues for a Trace-Scheduling Compiler, Yale University, December 1984.

- *Douglas Baldwin*. Automatic Evaluation of Design Choices in Digital Controller Design, Yale University, May 1985.

(Representative) Patents and University Grants:

- Patent Number: US5710912; Jan. 20, 1998; METHOD AND APPARATUS FOR ENABLING A COMPUTER SYSTEM TO ADJUST FOR LATENCY ASSUMPTIONS; Schlansker, Michael S; Rau, B. Ramakrishna; Gupta, Rajiv; Fisher, Joseph A.

- Patent Number: US5870576; Feb. 09, 1999; METHOD AND APPARATUS FOR STORING AND EXPANDING VARIABLE-LENGTH PROGRAM INSTRUCTIONS UPON DETECTION OF A MISS CONDITION WITHIN AN INSTRUCTION CACHE CONTAINING POINTERS TO COMPRESSED INSTRUCTIONS FOR WIDE INSTRUCTION WORD PROCESSOR ARCHITECTURES; Faraboschi, Paolo; Fisher, Joseph A.

- Patent Number: US6026479; Feb. 15, 2000; APPARATUS AND METHOD FOR EFFICIENT SWITCHING OF CPU MODE BETWEEN REGIONS OF HIGH INSTRUCTION LEVEL PARALLISM AND LOW INSTRUCTION LEVEL PARALLISM IN COMPUTER PROGRAMS; Fisher, Joseph A.; Faraboschi, Paolo; Emerson, Paul G.; Raje, Prasad A.

- Patent Number: US6122708; Sep. 19, 2000; DATA CACHE FOR USE WITH STREAMING DATA; Faraboschi, Paolo; Fisher, Joseph A.

- Patent Number: US7,051,340; May 23, 2006; SYSTEM AND METHOD FOR ISOLATING APPLICATIONS FROM EACH OTHER; Fisher, Joseph A; Lain, Antonio.

- National Science Foundation grant MCS-81-06181. An Attached Processor Systems Laboratory. $2,658,560. October 1981 - September 1986. Significant participant in obtaining and utilizing this department-wide Coordinated Experimental Research grant.
- Patent Number: US7,194,732; March 20, 2007; SYSTEM AND METHOD FOR FACILITATING PROFILING AN APPLICATION. Fisher, Joseph A.; Desoli, Giuseppe.

- National Science Foundation grant MCS-81-07646. The extension and application of global compaction techniques for horizontal scientific code. $94,599. July 1981 - December 1983.

- National Science Foundation grant MCS-83-08988. The extension and application of global compaction techniques for horizontal scientific code. $110,967. Renewal of MCS-81-07646. January 1984-December 1985.

- Several other university grants.

Personal Information:

Born July 22, 1946, Bronx, NY

Married (since 1967) to Elizabeth Fisher,

2 Children